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Description

Radio Receiver Supporting Multiple Modulation Formats with a Single Pair of ADCs

Cross Reference To Related Applications

[0001] This application claims the benefit of U.S. Provisional Application No. 60/483,115, filed 06/30/2003, and included herein by reference.

Background of Invention

[0002] 1. Field of the Invention

[0003] The present invention relates to a radio receiver, and more particularly, to a radio receiver that is capable of supporting multiple modulation formats with a single pair of analog to digital converters (ADCs).

[0004] 2. Description of the Prior Art

[0005] This is the age of radio communications. Around the world, cell phones are now one of the most common pieces of equipment to be found among the general pub-

lic. Wireless LAN (WLAN) is an acknowledged trend for business and consumer networking environments. The mobility enabled by wireless connections has dramatically changed and improved the lives of ordinary people. However, there is no universal standard for wireless modulation formats. For example, there are DECT, GSM-900, GSM-1800, WCDMA, and CDMA2000 systems for mobile telephony. Another situation is that there may be multiple modes within a standard. For example, there are OFDM modes and DSSS/CCK modes within the IEEE 802.11g standard. For mobile telephony systems base stations supporting multiple formats, signals of different standards need to be dealt with simultaneously. On the other hand, on the mobile station end, only one signal standard needs to be supported at the same time. For example, a base station that supports both GSM-1800 and WCDMA standards needs to deal simultaneously with signals modulated according to these formats. But a cell phone needs to receive or transmit signals of only one standard at one time.

[0006] The IEEE 802.11 WLAN standard provides a number of physical layer options in terms of data rates, modulation types and spreading spectrum technologies. Please refer

to Fig.1. Fig.1 illustrates provided data rates, sample rates, carrier frequencies and modulation types for various modes of IEEE WLAN standard. An extension of the IEEE 802.11 standard, namely IEEE 802.11a, defines requirements for a physical layer operating in the 5 GHz frequency and data rates ranging from 6Mps to 54Mps. IEEE 802.11a defines a physical layer based on the orthogonal frequency division multiplexing (OFDM) modulation scheme. A second extension, IEEE 802.11b, defines a set of physical layers' specifications operating in the 2.4GHz ISM frequency band up to 11 Mps. The direct sequence spread spectrum/complementary code keying (DSSS/CCK) physical layer is one of the three physical layers supported in the IEEE 802.11 standard and uses the 2.4GHz frequency band as the RF transmission media.

[0007] The IEEE standard committee has created a working group, TGg, with the mission of developing a higher speed PHY extension to the 802.1lb standard. The 802.11g standard will be compatible with the IEEE 802.11 MAC and will implement all mandatory portions of the IEEE 802.11b PHY standard. A part of the scope of TGg is to provide a wireless LAN standard where stations communicating in OFDM modulation and legacy stations com-

municating in DSSS/CCK modulation coexist and communicate with each other.

[0008] In a multiple mode standard, like IEEE 802.11g, signals of both the OFDM mode and the DSSS/CCK mode need to be dealt with, but only one mode can be performed at a time. All of these standards have been extensively adopted and have their own features and market niches. As a result, systems supporting multiple modulation formats are highly desirable.

[0009] Recently, technological advances in the design of programmable computing devices have made possible the real-time processing of algorithms formerly implemented by ASIC circuits, and this is especially true in the field of telecommunications. Thus, the complexity of transceivers can be partly moved from hardware to software. Moreover, due to the high level of reconfigurability, improved algorithms or newer versions of the transmission standards can be downloaded to the terminal, avoiding the need for hardware upgrades. Under this scenario, the adoption of a single user terminal, capable of interfacing with different transmission standards, opens the door to an enlarged set of services that can be delivered to the end user, with complete independence of the air interface

if proper techniques are chosen. For example, there are now available dual-system or even tri-system cell phones. There also exist IEEE 802.11g WLAN cards supporting both the OFDM DSSS/CCK modes.

[0010] Please refer to Fig.2. Fig.2 is a block diagram of a dual-system receiver R1 according to the prior art. Receiver R1 is a zero-IF radio architectured receiver for a mobile phone supporting both GSM-1800 and FDD WCDMA standards. The two systems operate in different radio frequency bands and at different data rates. Because of the different radio frequency bands, two radio frequency (RF) modules 10 and 20 are required to complete band selection, low noise amplification, down-conversion, and channel selection, as some of these functions are performed by frequency-selective components. Because the data rates of the two standards are different, and the modulations have an I/Q structure, two pairs of analog to digital converters (ADCs) 12 and 22 are adopted to sample the analog signals. The respective sampling rates of the two pairs of ADCs are in accordance with the modulation formats for GSM-1800 and the FDD WCDMA standard. Two baseband processing modules 14 and 24 are respectively electrically connected to the two pairs of ADCs 12, 22, and

each takes responsibility for performing detection, demodulation, time and frequency synchronization, decoding, and de-scrambling of signals of the respective predetermined standard.

[0011] Please refer to Fig.3. Fig.3 is a block diagram of another two-standard receiver R2 according to the prior art. Receiver R2 is a zero-IF radio architectured receiver for a WLAN card supporting IEEE 802.11g standard. As mentioned above, there are OFDM modes and DSSS/CCK modes within the IEEE 802.11g standard. The radio frequency bands of the two modes are the same, but the modulation formats and data rates are different. Since the radio frequency bands are the same, the RF module 30 is shared by the two modes. As I/Q structures are adopted in each of the modes, electrically connected to the RF module 30 are two pairs of ADCs 32 and 42. The two pairs of ADCs are capable of sampling the analog signals, and the sampling rate of each ADC pair corresponds to the data rate of the respective predetermined mode. Similarly, two baseband processing modules 34 and 44 are respectively electrically connected to the two ADCs 32, 42, providing functionality like that of the baseband processing modules 14 and 24 in receiver R1.

[0012] It is easily seen that there are duplicated analog circuits, especially the ADC circuits, in a receiver supporting multiple modulation formats of the prior art. The ADC circuits usually have very complicate configuration, and the area occupied by these circuits can be relatively large. Hence, the ADCs present a severe drawback in the design and manufacture of integrated circuits. The larger the area of a circuit is, the higher the total cost becomes. In addition, in a user terminal supporting multiple standards or multi-mode standards, only one signal modulation format needs to be handled at one time. There is no need to waste power on paths other than that which is receiving or transmitting the signals.

SUMMARY OF INVENTION

[0013] It is therefore a primary objective of the claimed invention to provide a radio receiver that can support multiple modulation formats with a single pair of ADCs and a power control module.

[0014] Briefly described, the claimed invention discloses a radio receiver capable of supporting a plurality of modulation formats. The radio receiver comprises an ADC electrically connected to an RF module for processing output signals of the RF module, a plurality of baseband processing

modules electrically connected to the ADC, and a power control module electrically connected to each of the plurality of baseband processing modules. Each of the baseband processing modules is capable of performing detection, demodulation, time and frequency synchronization, decoding, and de-scrambling of signals of a respective predetermined modulation format among the plurality of modulation formats. At least one of the baseband processing modules further comprises a rate converter respectively electrically connected to the ADC for converting a data rate of signals output from the ADC to a data rate of the corresponding predetermined modulation format. The power control module is electrically connected to each of the baseband processing modules, and is capable of controlling power to the baseband processing modules according to first signals respectively received from each of the baseband processing modules.

[0015] The claimed invention further discloses a radio receiver capable of supporting a plurality of modulation formats. The radio receiver comprises an ADC electrically connected to the RF module for processing the output signals of the RF module, and a plurality of baseband processing modules electrically connected to the ADC. Each of the

baseband processing modules is capable of performing detection, demodulation, time and frequency synchronization, decoding, and de-scrambling of signals of a respective predetermined modulation format among the plurality of modulation formats. At least one of the baseband processing modules further comprises a rate converter respectively electrically connected to the ADC for converting a data rate of signals output from the ADC to a data rate of the corresponding predetermined modulation format.

[0016] It is an advantage of the present invention that use of the rate converter enables elimination of a corresponding pair of ADCs. As rate converters are considerably easier to implement than ADCs, a significant saving in circuit complexity, and hence area, is obtained. This results in lower overall manufacturing costs of the radio receiver. Furthermore, the use of the power control module avoids wasting power on paths other than the path that is receiving or transmitting signals, which can lead to longer battery life.

[0017] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various fig-

ures and drawings.

Brief Description of Drawings

[0018] Fig.1 illustrates provided data rates, sample rates, carrier frequencies and modulation types for various modes of IEEE WLAN standard.

[0019] Fig.2 is a block diagram of a prior art multi-mode receiver having a zero-IF structure supporting different radio frequency bands and data rates.

[0020] Fig.3 is a block diagram of a prior art multi-mode receiver having a zero-IF structure supporting standards with which the radio frequency bands are close but the data rates are different.

[0021] Fig.4 is a block diagram of a present invention multi-mode receiver having a power control and a zero-IF structure module that supports standards having different radio frequency bands and data rates.

[0022] Fig.5 is a block diagram of a present invention multi-mode receiver having a power control module and a zero-IF structure that supports standards in which the radio frequency bands are close to one another but the data rates are different.

[0023] Fig.6 is a block diagram of a dual mode receiver according to the present invention.

[0024] Fig.7 is a block diagram of a present invention multi-standard receiver having a zero-IF structure that supports standards having different radio frequency bands and data rates.

[0025] Fig.8 is a block diagram of a present invention multi-standard receiver having a zero-IF structure that supports standards in which the radio frequency bands are close to one another but the data rates are different.

[0026] Fig. 9 is a block diagram schematically showing an SRC.

[0027] Fig. 10 is a view for explaining the operating characteristics of the SRC in Fig.9.

DETAILED DESCRIPTION

[0028] The primary reason for adopting multiple ADC pairs in a system supporting a plurality of modulation formats according to the prior art is that the data rates of the different modes or different standards are not the same. Each of the modes or standards needs to adopt an ADC pair having a predetermined sampling rate that matches the sampling rate of that mode or standard. Taking IEEE 802.11g, which is a multi-mode standard, as an example, if we want a WLAN card to support the IEEE 802.11g standard, then we have to deal with a 64QAM modulation for-

mat signal with a 20MHz data rate for the OFDM mode, and a QPSK modulation format signal with a 22MHz data rate for the DSSS/CCK mode, but only for one mode in a time. Similarly, in a multi-system cell phone supporting both GSM-1800 and WCDMA mobile telephony systems, both of the two modulation formats need to be dealt with, but the signals of different types of modulation formats are not utilized at the same time. The data rates of the two modes within the IEEE 802.11g standard or the data rates of GSM-1800 and WCDMA systems are different. Therefore, respective ADC pairs of different sampling rates are needed for the IEEE 802.11g WLAN card and the dual-system cell phone supporting both GSM-1800 and FDD-WCDMA according to the prior art.

[0029] In the present invention, only one ADC (or ADC pair) is adopted to implement the multi-mode or multi-standard radio receiver. A rate converter (or rate converter pair) is further provided in at least one of the baseband processing modules to convert the data rate of the signals sampled by the ADC (or ADC pair). In this manner, the data rates of signals for each modulation format are all converted to the predetermined rates suitable for that format, and the baseband processing modules can therefore func-

tion correctly. There is further provided a power control module in the present invention to reduce the power consumption of the baseband processing modules other than the one that is receiving or transmitting signals, since there is always only one signal modulation format processed at one time.

[0030] First Embodiment:

[0031] Please refer to Fig.4. Fig.4 is a block diagram of a multi-standard receiver R3 according to the present invention. The receiver R3 is a zero-IF radio architectured receiver for a dual-system cell phone supporting both GSM-1800 and FDD-WCDMA standards. The radio frequency bands of the two systems are different, and the data rates are 200KHz and 3.84MHz, respectively. For the different radio frequency bands, radio frequency (RF) modules 50 and 60 are utilized to complete band selection, low noise amplification, down-conversion, and channel selection. The RF modules 50 and 60 are electrically connected to the same pair of ADCs 52. The sampling rate of the ADCs is chosen to be 7.68MHz, which is twice the sampling rate of the highest modulation format data rate. By doubling the greatest data rate as the sampling rate, proper sampling is assured for all modulation format data rates. Two base-

band processing modules 54 and 64 are electrically connected to the pair of ADCs 52. The baseband processing module 54 takes the responsibility of performing detection, demodulation, time and frequency synchronization, decoding, and de-scrambling of signals modulated for the FDD-WCDMA standard. The data rate of the signal sampled by the ADC pair 52 is twice the data rate of the FDD-WCDMA standard, and is therefore appropriate for the baseband processing module 54 to perform its various functions. On the other hand, the data rate of the signal sampled by the ADC pair 52 is not appropriate for the baseband processing module 64. To convert the data rate, the baseband processing module 64 further comprises a pair of rate converters 66 electrically connected to the pair of ADCs 52 for converting the data rate of signals output from the pair of ADCs 52 to the data rate suitable for the GSM-1800 standard (i.e., 400KHz). The most common structures for the rate converters 66 are Farrow Interpolators or Decimation Filters. The baseband processing module 64 is also responsible for performing detection, demodulation, time and frequency synchronization, decoding, and de-scrambling of signals modulated under the MSK format of the GSM-1800 standard. Since the

7.68MHz data rate output by the ADC pair 52 is converted to a 400KHz data rate suitable for the GSM-1800 baseband processing module 64, the tasks of the baseband processing module 64 can be performed correctly. When a first baseband processing module 54, 64 detects signals of the respective predetermined format of the first baseband processing module 54, 64, it sends a first signal 54a, 64a to the power control module 58. The power control module 58 then turns all other baseband processing modules 64, 54 into a low power consumption mode except the first baseband processing module 54, 64, by way of control lines 58b, 58a. For example, if WCDMA signals are detected first, the baseband processing module 54 sends a first signal 54a to the power control module 58. In response, the power control module 58 puts the baseband processing module 64 into a low power mode by asserting a signal line 58b to save power, since there is no need to concurrently process GSM-1800 signals. When the transmission procedures of the baseband processing modules 54, 64 have completed (in the example, baseband module 54), the power control module 58 restores power to each baseband processing module 64, 54 (in the example, power is restored to baseband processing mod-

ule 64 by de-asserting the signal line 58b). Determination of when transmission procedures of the baseband processing modules 54, 64 are completed can be obtained, for example, from the first signal lines 54a, 64a and then waiting a predetermined period of time (which may be zero) before de-asserting all power control lines 58a, 58b.

[0032] Utilization of rate converters can bring distortion into signals. The modulation format of GSM-1800 is less prone to distortions than that of the FDD-WCDMA modulation format. That is, Minimum Shift Keying (MSK) is more robust than quadrature phase shift keying (QPSK). Consequently, another reason for choosing the sampling rate of the pair of ADCs 52 to be twice the data rate of the FDD-WCDMA standard is that it is consequently not necessary to adopt the rate converters in the baseband processing module 54, and hence there is no further distortion to the FDD-WCDMA signal. Also, according to the Nyquist theorem and as indicated above, the sampling rate of the ADCs 52 should be at least twice the highest data rate of all supported standards; that is, higher than or equal to 7.68MHz in this example.

[0033] In consider of circuit simplification, the sampling rate of the ADCs 52 can also be as the same as the highest data

rate among all support standards, such that the output of the ADCs 52 can be fed into the baseband processor with the highest data rate without a sample rate converter therebetween. In this embodiment, the sampling rate of the ADCs 52 can be chosen as 3.84MHz, which is the same as the data rate of the FDD-WCDMA standard. Under this assumption, the baseband processing module 54, which is for the FDD-WCDMA standard, does not need a sample rate converter since its date rate is the same as the sample rate of the ADCs 52. The baseband processing module 64, which is for the GSM-1800 standard, does require a sample rate converter to down convert the data rate from 3.84MHz to 200KHz.

[0034] Second Embodiment:

[0035] Fig.5 is a block diagram of a dual-mode receiver R4 according to the present invention. As shown in Fig. 5, the receiver R4 is a zero-IF radio architectured receiver for a user terminal supporting the IEEE 802.11g standard. The radio frequency bands for the OFDM mode and DSSS/CCK mode are both at 2.4GHz, and the data rates are 20MHz and 22MHz respectively. Since the radio frequency bands are the same, a single RF module 70 is utilized and shared for the two modulation standards. A pair of ADCs 72 is

electrically connected to the RF module 70. The modulation format of OFDM mode is 64QAM, and that of DSSS/CCK mode is QPSK. QPSK is lees prone to distortion than 64QAM. According to the principle for choosing the sampling rate of the ADCs as described above, the sampling rate of the ADCs is chosen to be at least twice the data rate of the QPSK format of DSSS/CCK mode, that is, 44MHz, and to be a multiple of the data rate of the 64QAM format of OFDM mode. Therefore, we choose 60MHz as the sampling rate of the pair of ADCs 72. Two baseband processing modules 74 and 84 are electrically connected to the pair of ADCs 72. The baseband processing module 74 is responsible for performing detection, demodulation, time and frequency synchronization, decoding, and de-scrambling of signals modulated under the 64QAM format for the OFDM mode. To convert the output data rate of the paired ADCs 72, the baseband processing module 84 further comprises a pair of rate converters 86 respectively electrically connected to the pair of ADCs 72 for converting the data rate of the signal output from the pair of ADCs 72 to a data rate suitable for the DSSS/CCK mode (i.e., 44MHz). The baseband processing module 84 is responsible for performing detection,

demodulation, time and frequency synchronization, de-coding, and de-scrambling of signals modulated under the QPSK format for the DSSS/CCK mode of the IEEE 802.11g standard. Since the data rate is converted, the task of the baseband processing module 84 can be per-formed correctly. When a first baseband processing mod-ule 74, 84 detects signals of the respective predetermined format of the first baseband processing module 74, 84, it sends a first signal 74a, 84a to the power control module 78. The power control module 78 then turns all other baseband processing modules 84, 74 into a low power mode, excepting the first baseband processing module 74, 84, by way of power control lines 78b, 78a. For exam-ple, if the user terminal first detects OFDM signals, the baseband processing module 74 sends a first signal 74a to the power control module 78. In response, the power control module 78 then forces the baseband processing module 84 into a low power mode by way of the signal line 78b to save power, since there is no need to simulta-neously process DSSS/CCK signals. When the transmission procedures of the baseband processing modules 74, 84 are completed, the power control module 78 turns on the power of each baseband processing module by de-

asserting the power control lines 78b, 78a.

[0036] The present invention uses only one ADC for non-I/Q structured signals, or one pair of ADCs for I/Q structured signals, in a radio receiver supporting multiple modulation formats. The sampling rate of the only one ADC or the only one pair of ADCs should satisfy two requirements: (1) The sampling rate should be at least twice the highest data rate of all supported standards; and (2) the data rate should be n times the data rate of the most complicated (or least distortion-tolerant) modulation format, where n is an integer. Having the data rate an integer multiple of the most complicated format helps to avoid utilizing a rate converter in the baseband processing module of the most complicated modulation format, and thus avoids signal distortion within that format. Second, the present invention uses a power control module. The power control module sets the baseband processing modules into a low power mode, except for the first baseband processing module that first detects signals, since there is no need for signals of more than one modulation format to be concurrently processed in the application of the present invention. The power control module turns on the power of each baseband processing module when transmission

procedures of the baseband processing modules are completed. In this manner, power is saved.

[0037] The dual mode receiver of the invention includes two kinds of modulation format, i.e. OFDM modulation for IEEE 802.11a standard and DSSS/CCK modulation for IEEE 802.11b standard. Please refer to Fig.6. Fig.6 is a block diagram of a dual mode receiver 500 according to the present invention. The dual mode receiver 500 includes a common ADC (analog-to-digital converter) 511, an AGC (automatic gain control) 516, an ACI (adjacent channel interference) filter 512, a first demodulation circuit 513 and a second demodulation circuit 514. The ADC 511 converts a baseband signal into a primary digital signal with a basic data rate of 40MHz. The AGC 516 adjusts the gain of the primary digital signal. The ACI filter 512 filters the adjusted primary digital signal to remove adjacent channel interference. The first demodulation circuit 513 comprises an SRC (sample rate converter) 5132 connected to the ACI filter 512, and a Farrow Interpolator 5134 connected to the SRC 5132. The SRC 5132 converts the primary digital signal with a basic data rate of 40MHz to a digital signal with a data rate of 22MHz. The Farrow Interpolator 5134 then performs timing recovery to synchronize the digital

signal. The second demodulation circuit 514 comprises a Farrow Interpolator and Decimator 5142 for converting the primary digital signal with a basic data rate of 40MHz to a digital signal with a data rate of 20MHz. The digital signal with a data rate of 20MHz is generated by decimating the primary digital signal with a basic data rate of 40MHz, not by sampling because the Farrow interpolator and decimator 5142 can decimate an input signal whose frequency is an integer multiple of the frequency of an output signal generated by the Farrow interpolator and decimator 5142. Although in this embodiment, the SRC 5132 is used to convert the primary digital signal with a basic data rate of 40MHz to a digital signal with a data rate of 22MHz, the SRC 5132 can be ignored so that the ACI filter 512 can directly input the primary digital signal with a basic data rate of 40MHz to the Farrow interpolator 5134.

[0038] Third Embodiment:

[0039] Please refer to Fig.7. Fig.7 shows an embodiment for a multi-standard receiver R5 of the present invention. Please refer to Fig.7. Fig.7 is a block diagram of a multi-standard receiver R5 according to the present invention. The receiver R5 is a zero-IF radio architectured receiver

for a PDA or other computing platform equipped with a WLAN card supporting the IEEE 802.11a standard, and capable of providing household appliance remote control functionality via the BLUETOOTH standard. The radio frequency bands of the two systems are 5.0GHz and 2.4GHZ, and the data rates are 20MHz and 1MHz. For the different radio frequency bands, radio frequency (RF) module 150 and 160 are utilized to complete band selection, low noise amplification, down-conversion, and channel selection. The two RF modules 150, 160 are electrically connected to the same pair of ADCs 152. The sampling rate of the ADCs is chosen to be 40MHz, which is twice the sampling rate of the highest modulation format data rate. By doubling the greatest data rate as the sampling rate, proper sampling is assured for all modulation format data rates. Two baseband processing modules 154 and 164 are electrically connected to the pair of ADCs 152. The baseband processing module 154 takes the responsibility of performing detection, demodulation, time and frequency synchronization, decoding, and de-scrambling of signals modulated with the 64QAM format for the 802.11a standard. The data rate of the signal sampled by the ADC pair is twice the data rate of the IEEE 802.11a standard, and is

therefore appropriate for the baseband processing module 154 in performing its various functions. On the other hand, the data rate of the signal sampled by the ADC pair 152 is not appropriate for the baseband processing module 164. To convert the data rate, the baseband processing module 164 further comprises a pair of rate converters 166 electrically connected to the pair of ADCs 152 for converting the data rate of signals output from the pair of ADCs 152, to a data rate suitable for the BLUETOOTH standard (i.e., 2MHz). The most common forms of rate converters are the Farrow Interpolator and the Decimation Filter. The baseband processing module 64 is also responsible for performing detection, demodulation, time and frequency synchronization, decoding, and descrambling of signals modulated under the FSK format of the BLUETOOTH standard. Since the 40MHz data rate output by the ADC pair 152 is converted to a 2MHz data rate suitable for the BLUETOOTH baseband processing module 164, the tasks of the baseband processing module 164 can be performed correctly. Further, the baseband processing modules 154 and 164 can process signals at the same time.

[0040] Utilization of rate converters can bring distortion into sig-

nals. The modulation format of IEEE 802.11a is more complicated than that of the BLUETOOTH modulation format. That is, 64QAM is more complicated then FSK. It is known that a simpler modulation format is more robust against distortion. Consequently, another reason for choosing the sampling rate of the pair of ADCs 152 to be twice the data rate of the IEEE 802.11a standard, is that it is consequently not necessary to adopt the rate converters in the baseband processing module 154, and hence there is no further distortion to the IEEE 802.11a signal. Also, according to the Nyquist theorem and as indicated above, the sampling rate of the ADCs 152 must be at least twice the highest data rate of all supported standards; that is, higher than or equal to 40MHz in this example.

[0041] Fourth Embodiment:

[0042] Please also refer to Fig.8. Fig.8 is a block diagram of another two-standard receiver R6 according to the present invention. The receiver R6 is a zero-IF radio architectured receiver for an access point (AP) supporting both IEEE 802.11b and BLUETOOTH systems. The radio frequency bands are both around 2.4GHz and the data rates are 22MHz and 1MHz respectively. Since the radio frequency bands are overlapping, a single RF module 170 is utilized

and shared for the two modulation standards. A pair of ADCs 172 is electrically connected to the RF module 170. The modulation format of IEEE 802.11b is QPSK, and that of BLUETOOTH is FSK. FSK is less prone to distortion than QPSK. According to the principle for choosing the sampling rate of the ADCs as described above, the sampling rate of the ADCs is chosen to be twice the data rate of IEEE 802.11b modulation format, that is, 44MHz. Two baseband processing modules 174 and 184 are electrically connected to the pair of ADCs 172. The baseband processing module 174 is responsible for performing detection, demodulation, time and frequency synchronization, decoding, and de-scrambling of signals modulated under the QPSK format for the IEEE 802.11b standard. To convert the output data rate of the paired ADCs 172, the baseband processing module 184 further comprises a pair of rate converters 186 respectively electrically connected to the pair of ADCs 172 for converting the data rate of the signal output from the pair of ADCs 172 to a data rate suitable for the BLUETOOTH standard (i.e., 2MHz). The baseband processing module 184 is responsible for performing detection, demodulation, time and frequency synchronization, decoding, and de-scrambling of signals

modulated under the FSK format for the BLUETOOTH standard. Since the data rate is converted, the task of the baseband processing module 184 can be performed correctly. Further, the baseband processing modules 174 and 184 can process signals at the same time.

[0043] In summary, the present invention uses only one ADC for non-I/Q structured signals or one pair of ADCs for I/Q structured signals in a radio receiver supporting multiple modulation formats. The sampling rate of the only one ADC or the only one pair of ADCs has to satisfy two requirements: (1) The sampling rate must be at least twice the highest data rate of all supported standards; and (2) the data rate should be n times the data rate of the most complicated modulation format, where n is an integer. Having the data rate an integer multiple of the most complicated format helps to avoid utilizing a rate converter in the baseband processing module of the most complicated modulation format, and thus avoids signal distortion.

[0044] Please refer to Fig. 9 and Fig. 10. Fig. 9 is a block diagram schematically showing an SRC (sample rate converter) 612. Fig. 10 is a view for explaining the operating characteristics of the SRC 612. The SRC 612 is used to convert a sample rate of data output from a first digital data pro-

cessing system 611 into a rate suitable for data processing in a second digital data processing system 613. The first digital data processing system 611 is for processing input data in accordance with clock signal CK1 of frequency f1; and the second digital data processing system 613 is for processing input data in accordance with clock signal CK2 of frequency f2, being different from frequency f1.

[0045] When the first digital data processing system 611 is applied to the input terminal I1 described above, it comprises an A/D conversion section for A/D converting an analog signal. The respective circuit components of the first digital data processing system 611 process input data using clock signal CK1, having frequency f1, and output digital data of f2 rate as a system output. In this application, the second digital data processing system 613 comprises an interpolating circuit for processing input data using clock signal CK2, having a frequency of f2.

[0046] The operation principle of SRC 612 will now be described with reference to Fig. 10. Reference symbols Xn and Xn+1 denote Xnth and (Xn+ 1)th data output from first digital data processing system 611. Data Xn and Xn+1 are synchronized with clock signal CK1. In order to supply these

data to system 613, which is operated in response to clock CK2, data Yn can be obtained at a timing of phase θ2 of clock signal CK2, and supplied to system 613. For this purpose, data Xn and Xn+1 can be linearly interpolated. This interpolation coefficient can be obtained by obtaining the phase relationship between clock signals CK1 and CK2.

[0047] In contrast to the prior art, the present invention radio receiver R3, R4 can support multiple I/Q modulation formats with a single pair of ADCs so that the circuit has a reduced complexity, the area of the circuit is reduced, and costs are thereby decreased. In addition, the present invention provides a power control module that forces unnecessary baseband processing modules into a low-power state, thereby conserving power. Further, the present invention radio receiver R5, R6 can support multiple modulation formats with a single pair of ADCs so that the circuit has a reduced complexity, the area of the circuit is reduced and costs are thereby decreased.

[0048] Those skilled in the art will readily observe that numerous modifications and alterations of the method and device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be con-

strued as limited only by the metes and bounds of the appended claims.